

Year & Sem: E1S2	Course Code: EC1203	Course Name: Digital Electronic Circuits	No. of Credits: 4	L 2	T&PS 2	P 0
Unit-I: Number Systems & Codes: Review of number systems: Digital systems, Binary, Octal & Hexadecimal Numbering systems, Number base conversions, binary arithmetic, complements of numbers, signed binary numbers, Binary codes: weighted & Non-weighted, error detecting & error correcting codes –hamming code and other codes. Boolean Algebra & Logic Gates: Boolean Algebra-Basic definition, Basic Logic operations, Basic theorems and properties, Truth tables, Boolean Functions, Representation of Boolean functions: Canonical & Standard forms, Other logic operations, Digital Logic gates, Universal gates. Unit-II: Gate Level Minimization: Algebraic simplification of Boolean expressions, the map method, four variable K-map, five variable K-map, Prime implicants, POS & SOP Simplification, Don't care conditions, Tabular Method- Simplification of Boolean function using tabulation Method, two level and multi-level NAND & NOR Implementation, Other two level Implementation circuits, Ex-OR Function and properties. Unit-III: Combinational Circuits: Combinational circuits, Analysis & Synthesis (Design) procedure, Design using conventional logic gates: Binary Adder-subtractor- Decimal Adder-Binary Multiplier- Magnitude comparator- Parity generators and checkers- Code Converters; Hazards; Decoder, Encoders, Multiplexers, Demultiplexer, Logic Design using MSI Components. Unit-IV: Synchronous Sequential Circuits: Sequential Circuits, Latches, Flips-Flops –Level and Edge triggering, Master- Slave Flip-flops & Edge triggered Flip-flops, Characteristic table and equation, Excitation table, Flip-flop conversions. Analysis of synchronous sequential circuits, State Reduction & Assignment, Design procedure of synchronous sequential circuits, Design examples: Serial binary adder-sequence detector. Unit-V: Shift Registers & Counters: Registers, Shift Registers: SISO, SIPO, PISO, PIPO & universal shift registers, Applications, Counters: Ripple Counters, Synchronous counters, other counters and Applications of counters. Finite State Machines: Introduction- General Model of FSM, Classifications of FSM (Mealy & Moore Models), Design of FSM, Design examples, Capabilities and limitations of FSM Unit-VI: Memory and Programmable Logic: Introduction, Random Access Memory, Memory Decoding, Read Only Memory, Programmable Logic Array, Programmable Array Logic, Sequential Programmable devices, Complex Programmable logic devices, Field Programmable Gate Arrays. References/Text Books: 1.M. Morris Mano & Michel D. Ciletti, "Digital Design: With an Introduction to Verilog HDL", 5th Edition, Pearson / PHI Publishers, 2013 3.Stephen Brown & Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design", 3rd Edition, McGraw Hill, 2013. 4.Ronald J. Tocci & Neal S. Widmer, "Digital Systems Principles and Applications", Pearson,						

10th Edition, 2011

1. Zvi Kohavi & Nirah K.Jha, “Switching theory and Finite Automata Theory” , 3rd Edition, Cambridge university press, 2010.
2. Anil K Maini, “Digital Electronics: Principles and Integrated Circuits”, 1st edition, John Wiley & Sons, 2007

Lecture Plan: Unit-I & -II syllabus for MID-I, Unit-III & -IV syllabus for MID-II and Unit-V & -VI syllabus for MID-III examinations.

Video Lectures (Web Links):

- 1.
- 2.

Study Materials (Web Links):

- 1.
- 2.

Problems & Solutions (Web Links):

- 1.
- 2.

Assignments (Web Links):

- 1.
- 2.