

Year & Sem:	Course Code: EC3606	Course Name: Low Power VLSI Circuits and Systems	No. of Credits: 4	L 2	T&PS 2	P 0
UNIT-I: Basics of MOS circuits: MOS Transistor structure and device modeling , MOS Inverters, MOS Combinational Circuits - Different Logic Families UNIT-II: Sources of Power dissipation: Dynamic Power Dissipation, Short Circuit Power, Switching Power, Glitching Power, Static Power Dissipation, Degrees of Freedom UNIT-III: Supply Voltage Scaling Approaches: Device feature size scaling, Multi-Vdd Circuits, Architectural level approaches: Parallelism, Pipelining, Voltage scaling using high-level transformations,Dynamic voltage scaling,Power Management UNIT-IV: Switched Capacitance Minimization Approaches: Hardware Software Tradeoff, Bus Encoding, Two's complement Vs Sign Magnitude, Architectural optimization, Clock Gating, Logic styles UNIT-V: Leakage Power minimization Approaches: Variable-threshold-voltage CMOS (VTCMOS) approach, Multi-threshold-voltage CMOS (MTCMOS) approach, Power gating, Transistor stacking, Dual-Vt assignment approach (DTCMOS) UNIT-VI: Special Topics: Adiabatic Switching Circuits, Battery-aware Synthesis, Variation tolerant design, CAD tools for low power synthesis References/Text Books: 1. Neil H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design, 2nd Edition, Addison Wesley (Indian reprint). 2. Bellamour, and M. I. Elmasri, Low Power VLSI CMOS Circuit Design, Kluwer Academic Press, 1995. 3. Anantha P. Chandrakasan and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers, 1995. 4. Kaushik Roy and Sharat C. Prasad, Low-Power CMOS VLSI Design, Wiley-Interscience, 2000. Lecture Plan: Unit-I & -II syllabus for MID-I, Unit-III & -IV syllabus for MID-II and Unit-V & -VI syllabus for MID-III examinations. Video Lectures (Web Links): 1. http://nptel.ac.in/courses/106105034/ 2. Study Materials (Web Links): 1. 2.						