

Year & Sem:	Course Code: EC4503	Course Name: Digital IC Design	No. of Credits: 4	L 2	T&PS 2	P 0
UNIT I: A Historical Perspective, Issues in Digital Integrated Circuit Design, Quality Metrics of a Digital Design, Cost of an Integrated Circuit, Functionality and Robustness, Performance, Power and Energy Consumption UNIT II: THE WIRE: Introduction, Interconnect Parameters — Capacitance, Resistance, and Inductance, Capacitance, Resistance, Inductance, Electrical Wire Models, The Ideal Wire, The Lumped Model, The Lumped RC model, The Distributed rc Line, The Transmission Line UNIT III: THE CMOS INVERTER: Introduction, The Static CMOS Inverter — An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter: The Static Behavior, Switching Threshold, Noise Margins, Performance of CMOS Inverter: The Dynamic Behavior, Computing the Capacitances, Propagation Delay: First-Order Analysis, Propagation Delay from a Design Perspective, Power, Energy, and Energy-Delay, Dynamic Power Consumption, Static Consumption UNIT IV: DESIGNING COMBINATIONAL LOGIC GATES IN CMOS: Introduction, Static CMOS Design, Complementary CMOS, Ratioed Logic, Pass-Transistor Logic, Dynamic CMOS Design, Dynamic Logic: Basic Principles, Speed and Power Dissipation of Dynamic Logic, Issues in Dynamic Design, Cascading Dynamic Gates, Perspectives, Designing Logic for Reduced Supply Voltages UNIT V: DESIGNING SEQUENTIAL LOGIC CIRCUITS: Introduction, Timing Metrics for Sequential Circuits, Classification of Memory Elements, Static Latches and Registers, The Bistability Principle, Multiplexer-Based Latches, Master-Slave Edge-Triggered Register, Low-Voltage Static Latches, Static SR Flip-Flops—Writing Data by Pure Force, Dynamic Latches and Registers, Dynamic Transmission-Gate Edge-triggered Registers, C2MOS—A Clock-Skew Insensitive Approach, True Single-Phase Clocked Register (TSPCR), Alternative Register Styles, Pulse Registers Sense-Amplifier Based, Registers, Pipelining: An approach to optimize sequential circuits, Latch- vs. Register-Based Pipelines, NORA-CMOS—A Logic Style for Pipelined Structures, Non-Bistable Sequential Circuits UNIT VI: DESIGNING MEMORY AND ARRAY STRUCTURES: Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories Nonvolatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers Voltage References, Drivers/Buffers, Timing and Control, Memory Reliability and Yield, Signal-To-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Data-retention dissipation References/Text Books: 1. Digital Integrated Circuits- A Design Perspective (Second Edition) by Jan M. Rabaey ,						

Anantha Chandrakasan and Borivoje Nikolic

Lecture Plan: Unit-I & -II syllabus for MID-I, Unit-III & -IV syllabus for MID-II and Unit-V & -VI syllabus for MID-III examinations.

Video Lectures (Web Links):

1. <https://www.youtube.com/playlist?list=PLB3i9IKhwBX8EEkgSy0AjaRFCmY2gBiQc>
- 2.

Study Materials (Web Links):

- 1.
- 2.

Problems & Solutions (Web Links):

- 1.
- 2.

Assignments (Web Links):

- 1.
- 2.